CMOS Analog VLSI Design

Roll no. 153079029

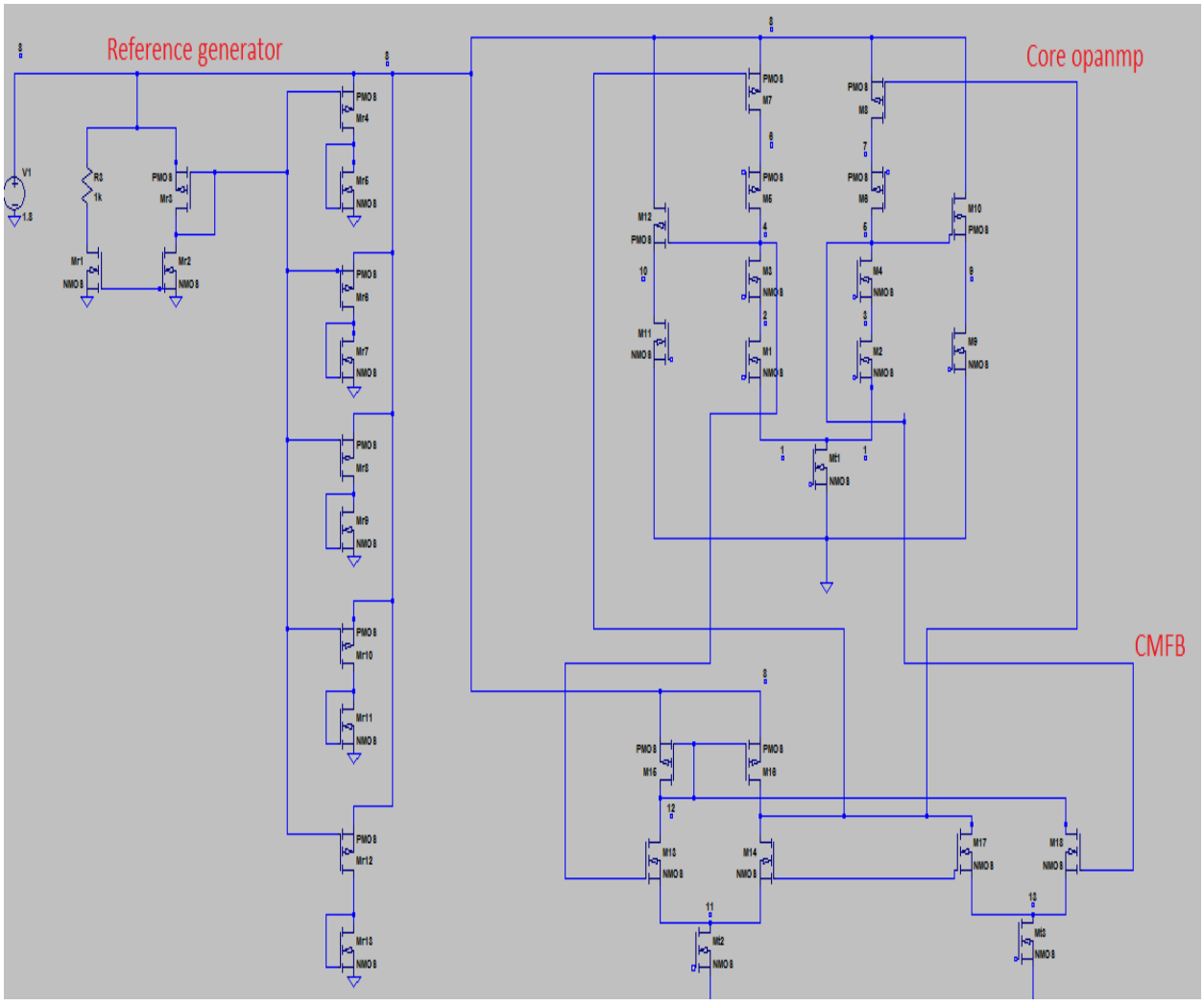
EE618

CMOS OpAmp Course Project

➢ Section 1:

Architecture : Telescopic two stage Op-Amp

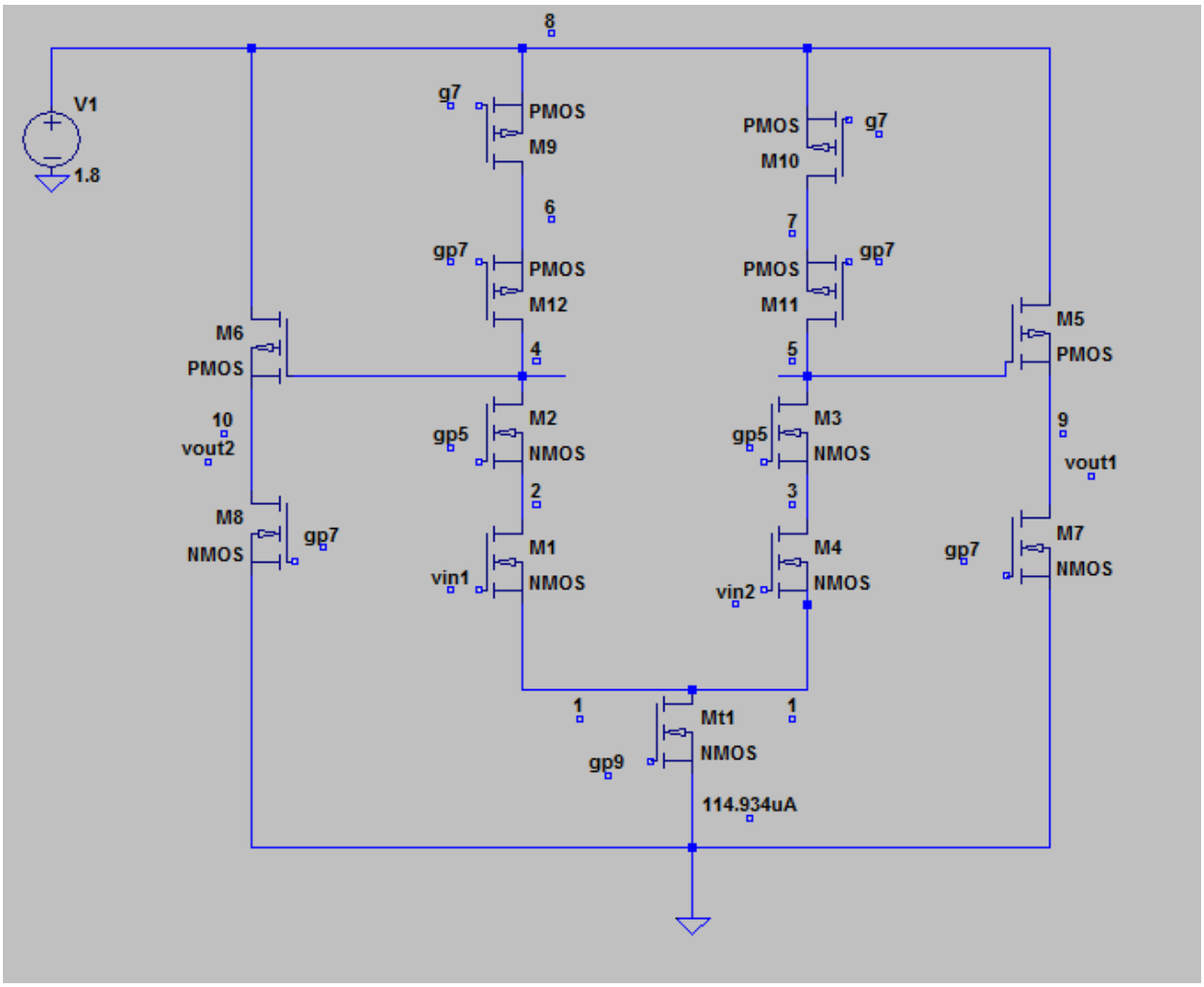
➢ Full schematic



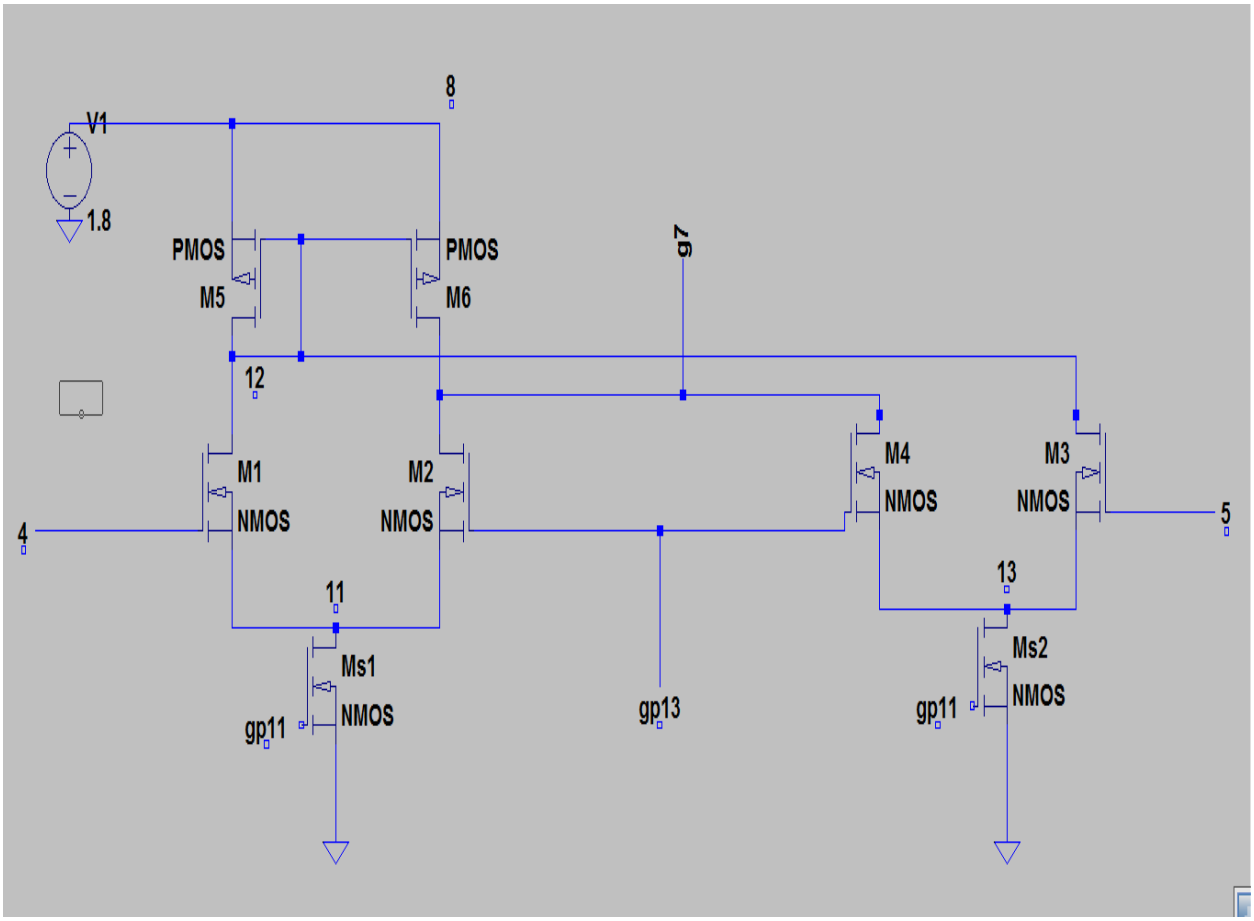
Core OpAmp

First stage: Telescopic

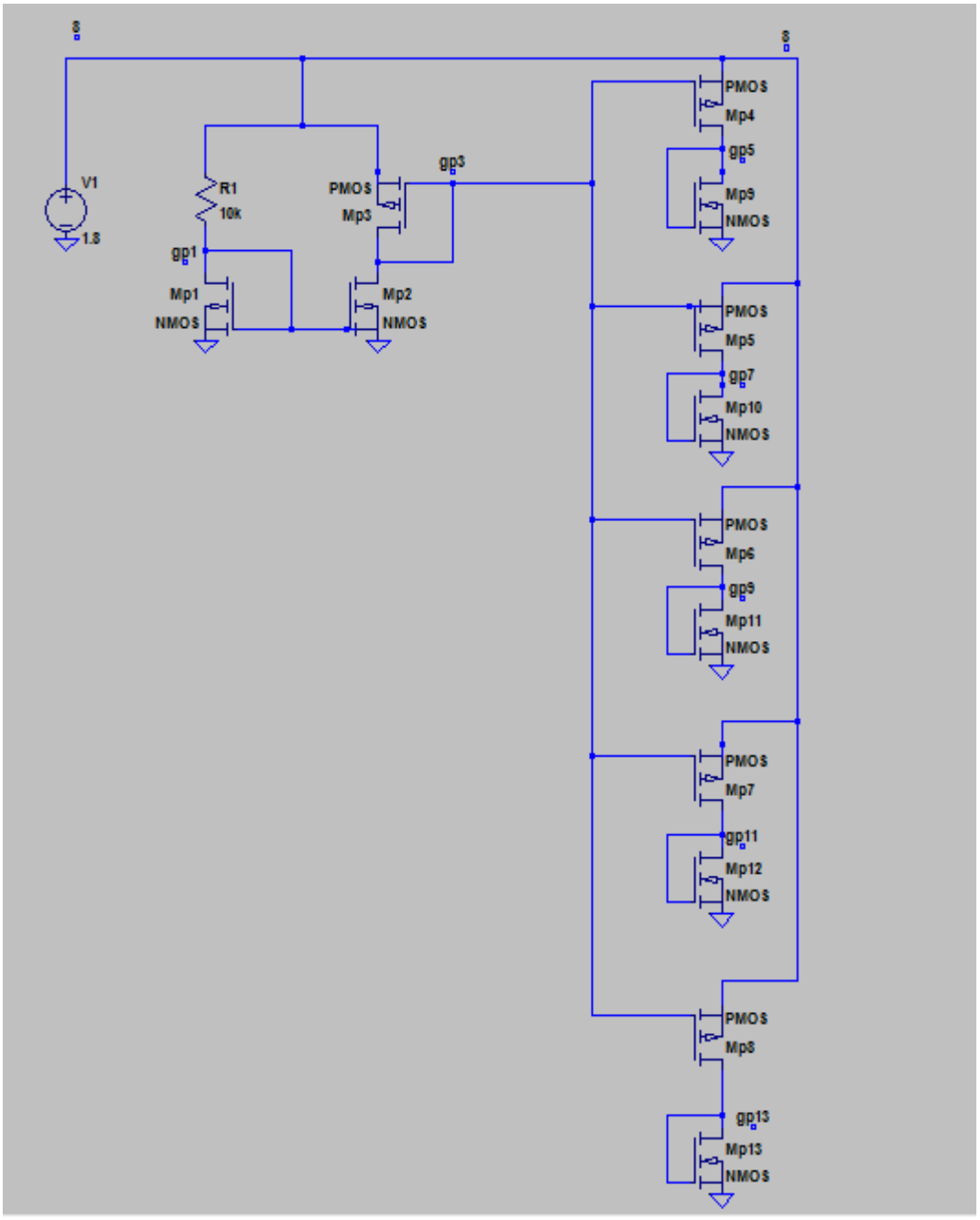
2nd Stage : Common Source stage



CMFB


8
V1
1.8
PMOS
M5
PMOS
M6
g7
12
M1
NMOS
M2
NMOS
M4
NMOS
M3
NMOS
4
5
11
13
Ms1
NMOS
gp11
gp13
Ms2
NMOS
gp11

Bias Generator



Section 2:

Abstract Design Flow

1> According to the design specification, telescopic opamp is used in the first stage and common source configuration is used in the second stage.

2> From Slew rate specification and by deciding compensation capacitor, the bias current requirement is fixed to ensure sufficient slewing period. The bias current of 2^{nd} stage is fixed nearly 5 times the first stage so that during slewing it does not load first stage and we can get better slew rate.

3> Gm1 can be found from wu from which input transistor overdrive can be decided.

4> From the input common mode specifications, we can decide overdrive voltages and over drive voltages of other upper MOSFETS

5> Once current and overdrive is known, biasing can be decided.

6> We need to ensure that C1<<Cc and C1<<Cl and for this we keep the W/L ratios minimum for transistors connected to the output of stage 1.

7> The dominant pole must be kept as close to origin so as to get wu of desired specification. This can be achieved by frequency compensation technique.

8> The Rz1,2 and Cc1,2 are used for frequency compensation but their introduction makes the system third order and may cause instability due to insufficient phase margin introduced due to third pole.

9> Therefore , pole 2 and zero cancellation is necessary to improve unity gain bandwidth as well as phase margin to desired specifications.

10> Rz1,2 must be high enough so that zero introduced by Cc1,2 is on the left half of s-plane so that stability can be ensured.

11> Pole 3 must be far away from Wu.

12> The CMFB should be designed with reasonably high gain to ensure less errors and make the output stage stable. Its open loop phase margin should be high enough to ensure stablilty at high frequency.

13> Reference generators are designed for stable voltage biasing to inputs of different MOSFETs. Current mirroring technique is used by chossig appropriate W/L ratios for the tail current source of 1^{st} , 2^{nd} stage and tail current and reference source of CMFB.

➢ Section 3:

Detailed Design flow of OpAmp

➢ The slew rate is given as:

Slew Rate ≥ 20 V/us

First Stage Bias Current

➢ **S.R. =** $\frac{Ibias\,1}{Cc}$

➢ C_L =5pF load capacitance is given and we know that **Cc≥ 0.3 *C_L**
So, choosing **Cc=2.5pF**

➢ Therefore , **I_{bias} ≥ 50 uA**

➢ Choosing **I_{bias} = 114uA for** the tail current source of the first stage to sufficient slew rate.

Second Stage Bias Current

➢ **S.R. =** $\frac{Ibias\,2}{Cc+CL}$

➢ I_{bias2} ≥ **150uA**

➢ Choosing **I_{bias2} = 572 uA**

W and L Values of Transistors

1> 1st Stage OpAmp

Name of transistors	W and L values
Ms	W=33.33um, L=1um
M1,2	W=50um, L=1um
M3,4	W=20.65um, L=1um
M5,6	W=33.6um, L=1um
M7,8	W=55.38um, L=1um

2nd Stage OpAmp

Name of transistors	W and L values
M9,11	W=20.1um, L=0.5um
M10,12	W=81um, L=0.3um

2> Common Mode Feedback (CMFB)

Name of transistors	W and L values
Ms2	W=15um, L=1um
M14,15	W=15um, L=1um
M16,17	W=25um, L=1um
Ms3	W=15um, L=1um
M18,19	W=25um, L=1um

3>Reference Generator

Name of transistors	W and L values
Mp1	W=2um, L=1um
Mp2	W=2um, L=1um
Mp3	W=8.7um, L=1um
Mp4	W=33.7um, L=1um
Mp5	W=2um, L=1um
Mp6	W=3.63um, L=1um
Mp7	W=2um, L=1um
Mp8	W=2um, L=1um
Mp9	W=5.1um, L=1um
Mp10	W=2um, L=1um
Mp11	W=8.5um, L=1um
Mp12	W=11.83um, L=1um
Mp13	W=2um, L=1um

Netlist of entire OpAmp Design:

********** First stage design **********

```
.include MOS.txt
Ms1 1 gp9 0 0 CMOSN L=1um W=33.33um as=2.88p ad=2.88p ps=16.72u pd=16.72u

M1 2 g1 1 1 CMOSN L=1um W=50um  as=10.8p ad=10.8p ps=780u pd=780u
M2 3 g2 1 1 CMOSN L=1um W=50um  as=10.8p ad=10.8p ps=780u pd=780u
M3 4 gp5 2 2 CMOSN L=1um W=20.65um as=4.4604p ad=4.4604p ps=25.5u pd=25.5u
M4 5 gp5 3 3 CMOSN L=1um W=20.65um  as=4.4604p ad=4.4604p ps=25.5u pd=25.5u

M5 4 gp3 6 6 CMOSP L=1um W=33.6um  as=7.2576p ad=7.2576p ps=41.04u pd=41.04u
M6 5 gp3 7 7 CMOSP L=1um W=33.6um  as=7.2576p ad=7.2576p ps=41.04u pd=41.04u
M7 6 g7 8 8 CMOSP L=1um W=55.38um  as=7.2576p ad=7.2576p ps=67.88u pd=67.88u
M8 7 g7 8 8 CMOSP L=1um W=55.38um  as=7.2576p ad=7.2576p ps=67.88u pd=67.88u

*RG1 4 n 1000G
*RG2 5 n 1000G
```

```
Vdd 8 0 dc 1.8

*Vbs1 gs1 0 dc 0.58
*Vb1 g1 0 dc 0.93 ac 1v
*Vb2 g2 0 dc 0.93
*Vb3 g3 0 dc 1.52
*Vb4 g4 0 dc 1.52

*Vb5 g5 0 dc 0.8
*Vb6 g6 0 dc 0.8
*Vb7 g7 0 dc 1.181
*Vb8 g8 0 dc 1.181

********** Second Stage Design **********

M9 9 gp7 0 0 CMOSN L=0.5um W=20.1um as=4.068p ad=4.068p ps=23.32u pd=23.32u
M10 9 5 8 8 CMOSP L=0.3um W=81um as=29.216p ad=29.216p ps=162.72u pd=162.72u
*Vb9 g9 0 dc 0.78

M11 10 gp7 0 0 CMOSN L=0.5um W=20.1um as=4.068p ad=4.068p ps=23.32u pd=23.32u
M12 10 4 8 8 CMOSP L=0.3um W=81um   as=29.232p ad=29.232p ps=162.72u pd=162.72u
*Vb11  g11 0 dc 0.78

Cl 9 10 5pF
cc1 x2 10 2.5pf
cc2 x1 9 2.5pf
Rz1 4 x2 1.9k
Rz2 5 x1 1.9k

********** CMFB design **********

MS2 11 gp11 0 0 CMOSN L=1um W=15um
M14 12 4 11 11 CMOSN L=1um W=15um
M15 g7 gp13 11 11 CMOSN L=1um W=15um
M16 12 12 8 8 CMOSP L=1um W=25um
M17 g7 12 8 8 CMOSP L=1um W=25um

*Vbs2 gs2 0 dc 0.54
*Vg14 g14 0 dc 1.101

*Vref ref 0 dc 1.103449

MS3 13 gp11 0 0 CMOSN L=1um W=15um
M18 12 5 13 13 CMOSN L=1um W=15um
M19 g7 gp13 13 13 CMOSN L=1um W=15um
*M20 14 14 8 8 CMOSP L=1um W=25um
```

```
*M21 g8 14 8 8 CMOSP L=1um W=25um

*Vbs3 gs3 0 dc 0.54
*Vg18 g18 0 dc 1.101

********** Reference Generator for bias voltages**********

mp1 gp1 gp1 0 0 cmosn l=1u w=2u
mp2 gp3 gp1 0 0 cmosn l=1u w=2u
mp3 gp3 gp3 8 8 cmosp l=1u w=8.7u
rp1 8 gp1 10k
vdd 8 0 1.8

**********MOS 3,4 bias 1.52

mp4 gp5 gp3 8 8 cmosp l=1u w=33.7u
mp5 gp5 gp5 0 0 cmosn l=1u w=2u

**********MOS 10,12 bias 0.78
mp6 gp7 gp3 8 8 cmosp l=1u w=3.63u
mp7 gp7 gp7 0 0 cmosn l=1u w=2u

**********Ms1 tail bias 0.58
mp8 gp9 gp3 8 8 cmosp l=1u w=2u
mp9 gp9 gp9 0 0 cmosn l=1u w=5.1u

**********CMFB tail ms2 ms3 bias 0.54
mp10 gp11 gp3 8 8 cmosp l=1u w=2u
mp11 gp11 gp11 0 0 cmosn l=1u w=8.5u

**********CMFB reference 1.103449
mp12 gp13 gp3 8 8 cmosp l=1u w=11.83u
mp13 gp13 gp13 0 0 cmosn l=1u w=2u

********************************************************************************
Rs1 sr1 g1 1meg
Rs2 sr2 g2 1meg
Rs3 g1 9 1meg
Rs4 g2 10 1meg

*Vsr1 sr1 0 pulse(0.775 1.225 1n 1n 1n 1u 2u)
*Vsr2 sr2 0 pulse(1.225 0.775 1n 1n 1n 1u 2u)
Vsr1 sr1 0 sin(0.93 0.4 1k 0 0)
Vsr2 sr2 0 sin(0.93 -0.4 1k 0 0)
.tran 0 4m

********************************************************************************
```

```
*.ac dec 100 100Hz 100G

.control
run

plot v(sr1) v(10,9)
*plot deriv(v(10,9))

*plot vdb(10,9) xlog
*plot vp(10,9) xlog
*plot vdb(4,5)
*op
*show
*print v(4) v(5) v(9) v(10)

.endc
.end
```

➢ Section 4:

1>Design of CMFB

- The biasing requirement of transistors M7 and M8 is 1.181V.
- The output bias voltage at nodes 4 and 5 is 1.103V
- Therefore, the reference voltage of CMFB is set to 1.103V which is made available from stable reference generator whereas the inputs to gate of M14 and M18 is made directly available from nodes 4 and 5.

  V_{ref} = 1.103V is applied to gate of 15 and M19.

  Vg14 is made available from node 4.

  Vg18 is made available from node 5.
- Current of CMFB is so chosen that it is low enough to get higher gain so that the output of opamp is stable w.r.t to variatons in dc input voltage.
  - Therefore, setting **I_{bias} =32 uA** for MS2 and MS3.

- **Common Mode Feedback (CMFB) W and L values.**

  Since we now know the values of current in each branch of CMFB and assuming overdrive values for each transistors, we obtain their W and L values.

  $$I_D = 0.5 * u_n * Cox * (W/L) * (V_{overdrive})^2$$

  Assuming L=1um

Name of transistors	W and L values
Ms2	W=15um, L=1um
M14,15	W=15um, L=1um
M16,17	W=25um, L=1um
Ms3	W=15um, L=1um
M18,19	W=25um, L=1um

Netlist of CMFB

```
.include MOS.txt
MS2 11 gs2 0 0 CMOSN L=1um W=15um
M14 12 g14 11 11 CMOSN L=1um W=15um
M15 g7 ref 11 11 CMOSN L=1um W=15um
M16 12 12 8 8 CMOSP L=1um W=25um
M17 g7 12 8 8 CMOSP L=1um W=25um
Vbs2 gs2 0 dc 0.54
Vg14 g14 0 dc 1.103449 ac 1
Vdd 8 0 1.8
Vref ref 0 dc 1.103449
MS3 13 gs3 0 0 CMOSN L=1um W=15um
M18 12 g18 13 13 CMOSN L=1um W=15um
M19 g7 ref 13 13 CMOSN L=1um W=15um
Vbs3 gs3 0 dc 0.54
Vg18 g18 0 dc 1.103449
.ac dec 100 100Hz 100G
.control
run
```

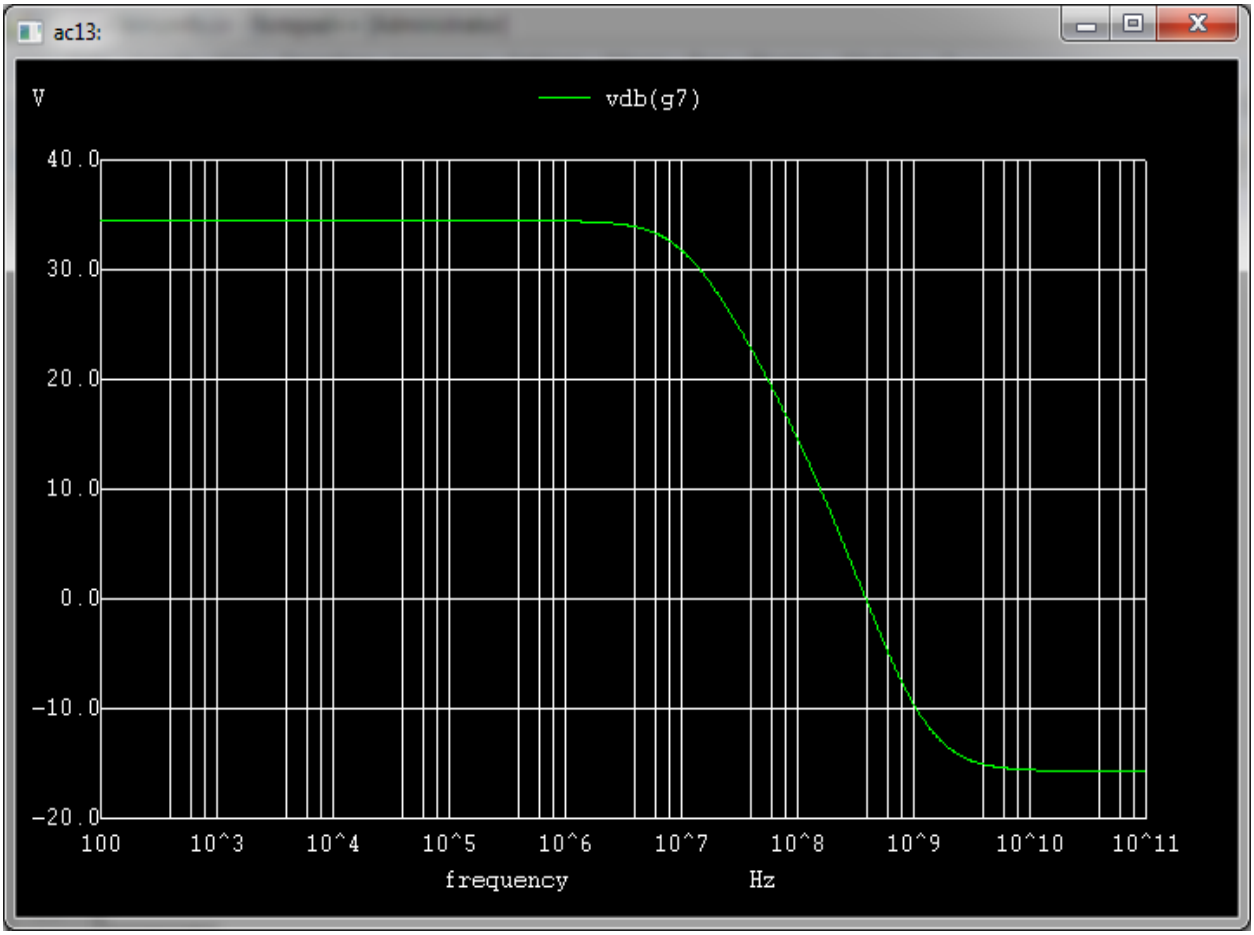
plot vdb(g7) xlog

plot vp(g7) xlog

.end

.end

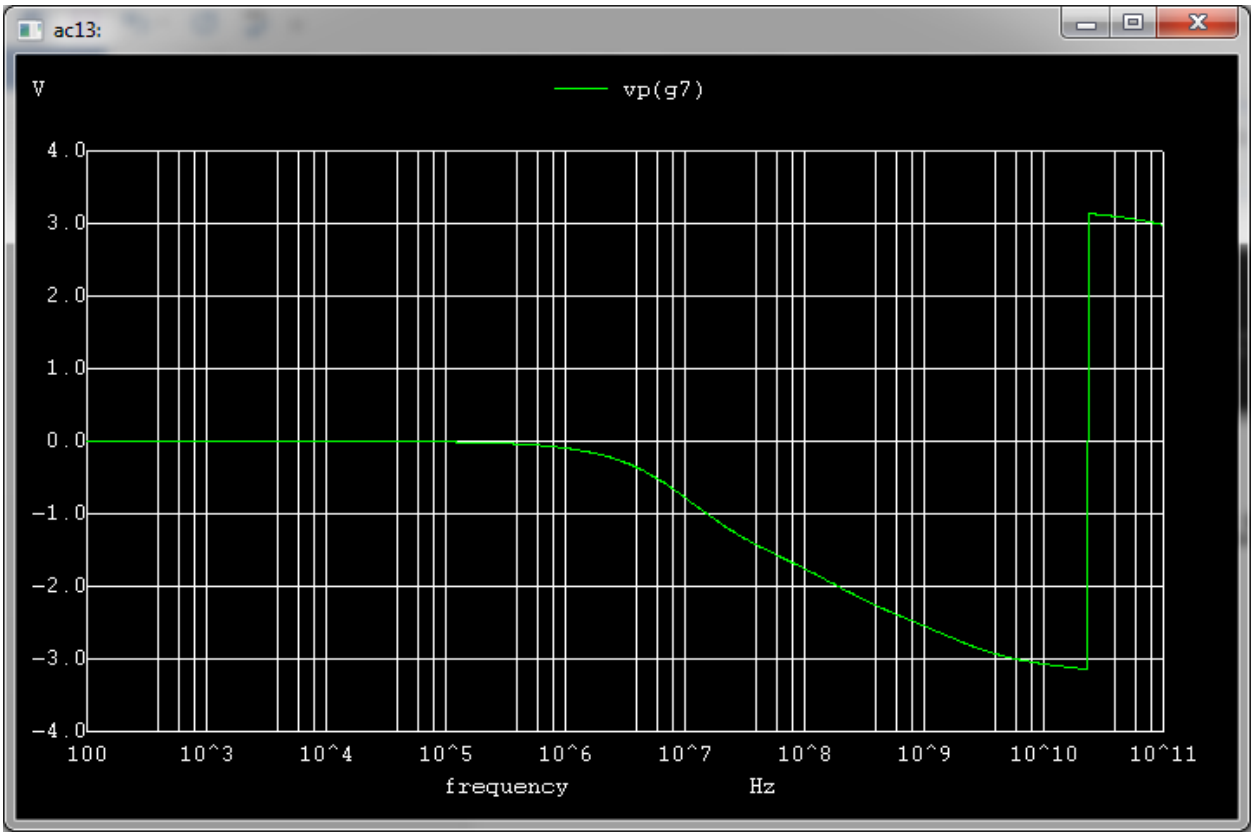
Gain Plot



Gain in dB for CMFB = 34.4828 dB = 52.98

Unity Gain Bandwidth of CMFB = 395 MHz

Phase Plot



Phase Margin of CMFB = 51.08

2>Design of Reference Generator

Name of transistors	W and L values
Mp1	W=2um, L=1um
Mp2	W=2um, L=1um
Mp3	W=8.7um, L=1um
Mp4	W=33.7um, L=1um
Mp5	W=2um, L=1um
Mp6	W=3.63um, L=1um
Mp7	W=2um, L=1um
Mp8	W=2um, L=1um
Mp9	W=5.1um, L=1um
Mp10	W=2um, L=1um
Mp11	W=8.5um, L=1um
Mp12	W=11.83um, L=1um
Mp13	W=2um, L=1um

Netlist for Reference Generator

.include MOS.txt

mp1 gp1 gp1 0 0 cmosn l=1u w=2u

mp2 gp3 gp1 0 0 cmosn l=1u w=2u

mp3 gp3 gp3 8 8 cmosp l=1u w=8.7u

rp1 8 gp1 10k

vdd 8 0 1.8

**********MOS 3,4 bias 1.52*

mp4 gp5 gp3 8 8 cmosp l=1u w=33.7u

mp5 gp5 gp5 0 0 cmosn l=1u w=2u

**********MOS 10,12 bias 0.78*

mp6 gp7 gp3 8 8 cmosp l=1u w=3.63u

mp7 gp7 gp7 0 0 cmosn l=1u w=2u

**********Ms1 tail bias 0.58*

mp8 gp9 gp3 8 8 cmosp l=1u w=2u

mp9 gp9 gp9 0 0 cmosn l=1u w=5.1u

**********CMFB tail ms2 ms3 bias 0.54*

mp10 gp11 gp3 8 8 cmosp l=1u w=2u

mp11 gp11 gp11 0 0 cmosn l=1u w=8.5u

**********CMFB reference 1.103449*

mp12 gp13 gp3 8 8 cmosp l=1u w=11.83u

mp13 gp13 gp13 0 0 cmosn l=1u w=2u

.control

run

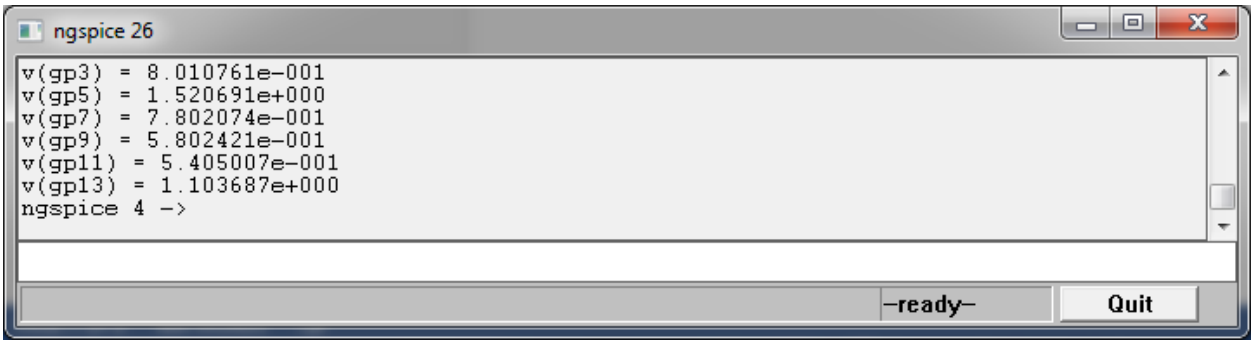
op

show

print v(gp3) v(gp5) v(gp7) v(gp9) v(gp11) v(gp13)

.endc

.end



The above netlist is run in ngspice and the result is shown above. All the voltages shown above are the bias voltages given to OpAmp and CMFB as specified in the netlist comments.

The voltages from reference generator is given to the gate of

- M5,M6
- M3,M4
- M10, M12
- MS1
- MS2, MS3
- M15 , M19

respectively according to above results.

➢ Section 5:

DC Simulaton results

DC operating points from ngspice simulation for all transistors are shown below as follows:

```
BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)
    device                  ms1
     model                 cmosn
         l                1e-006
         w             3.333e-005
         m                     1
        ad             2.88e-012
        as             2.88e-012
        pd             3.333e-005
        ps             3.333e-005
       nrd                     1
       nrs                     1
       off                     0
    nqsmod                     0
      gmbs           0.000369848
        gm             0.0013199
       gds          1.22988e-005
     vdsat              0.132815
       vth              0.411016
        id           0.000114934
       vbs          -0.000781553
       vgs              0.579461
       vds              0.427206
```

```
BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)
    device                    m3                    m2                    m1
     model                 cmosn                 cmosn                 cmosn
         l                1e-006                1e-006                1e-006
         w             2.065e-005                5e-005                5e-005
         m                     1                     1                     1
        ad          4.4604e-012           1.08e-011             1.08e-011
        as          4.4604e-012           1.08e-011             1.08e-011
        pd            2.55e-005               0.00078               0.00078
        ps            2.55e-005               0.00078               0.00078
       nrd                    1                     1                     1
       nrs                    1                     1                     1
       off                    0                     0                     0
    nqsmod                    0                     0                     0
      gmbs          0.000188884           0.000278433           0.000278433
        gm          0.000669936           0.000977315           0.000977315
       gds          6.6217e-005          6.04372e-006          6.04372e-006
     vdsat             0.124953             0.0855194             0.0855194
       vth             0.411789              0.410602              0.410602
        id          5.74671e-005          5.74671e-005          5.74671e-005
       vbs          -0.000390776          -0.000390776          -0.000390776
       vgs              0.567953               0.50084               0.50084
       vds              0.150744              0.522797              0.522797
```

BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)

device	m11	m9	m4
model	cmosn	cmosn	cmosn
l	5e-007	5e-007	1e-006
w	2.01e-005	2.01e-005	2.065e-005
m	1	1	1
ad	4.068e-012	4.068e-012	4.4604e-012
as	4.068e-012	4.068e-012	4.4604e-012
pd	2.332e-005	2.332e-005	2.55e-005
ps	2.332e-005	2.332e-005	2.55e-005
nrd	1	1	1
nrs	1	1	1
off	0	0	0
nqsmod	0	0	0
gmbs	0.00084982	0.00084982	0.000188884
gm	0.00315271	0.00315271	0.000669936
gds	3.25192e-005	3.25192e-005	6.6217e-005
vdsat	0.221149	0.221149	0.124953
vth	0.4442	0.4442	0.411789
id	0.000572616	0.000572616	5.74671e-005
vbs	-0.00389379	-0.00389379	-0.000390776
vgs	0.776314	0.776314	0.567953
vds	0.933626	0.933626	0.150744

BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)

device	m15	m14	ms2
model	cmosn	cmosn	cmosn
l	1e-006	1e-006	1e-006
w	1.5e-005	1.5e-005	1.5e-005
m	1	1	1
ad	0	0	0
as	0	0	0
pd	0	0	0
ps	0	0	0
nrd	1	1	1
nrs	1	1	1
off	0	0	0
nqsmod	0	0	0
gmbs	7.93639e-005	7.94237e-005	0.000126739
gm	0.000278229	0.000278443	0.000448928
gds	1.61626e-006	1.64103e-006	2.75938e-006
vdsat	0.0831455	0.0832072	0.108759
vth	0.410041	0.410111	0.410023
id	1.60451e-005	1.60647e-005	3.21098e-005
vbs	-0.000109107	-0.00010924	-0.000218347
vgs	0.495966	0.496152	0.540282
vds	0.592718	0.572937	0.607175

BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)

device	m19	m18	ms3
model	cmosn	cmosn	cmosn
l	1e-006	1e-006	1e-006
w	1.5e-005	1.5e-005	1.5e-005
m	1	1	1
ad	0	0	0
as	0	0	0
pd	1.5e-005	0	0
ps	1.5e-005	0	0
nrd	1	1	1
nrs	1	1	1
off	0	0	0
nqsmod	0	0	0
gmbs	7.93639e-005	7.94237e-005	0.000126739
gm	0.000278229	0.000278443	0.000448928
gds	1.61626e-006	1.64103e-006	2.75938e-006
vdsat	0.0831455	0.0832072	0.108759
vth	0.410041	0.410111	0.410023
id	1.60451e-005	1.60647e-005	3.21098e-005
vbs	-0.000109107	-0.00010924	-0.000218347
vgs	0.495966	0.496152	0.540282
vds	0.592718	0.572937	0.607175

BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)

device	mp5	mp2	mp1
model	cmosn	cmosn	cmosn
l	1e-006	1e-006	1e-006
w	2e-006	2e-006	2e-006
m	1	1	1
ad	0	0	0
as	0	0	0
pd	0	0	0
ps	0	0	0
nrd	1	1	1
nrs	1	1	1
off	0	0	0
nqsmod	0	0	0
gmbs	0.00010459	6.46148e-005	6.52268e-005
gm	0.000364027	0.000243678	0.000246329
gds	5.15779e-006	4.18925e-006	2.75366e-006
vdsat	0.668633	0.387939	0.388337
vth	0.40508	0.407336	0.406602
id	0.000243416	7.8986e-005	7.96625e-005
vbs	-0.00165523	-0.000537105	-0.000541705
vgs	1.51904	1.00284	1.00283
vds	1.51738	0.800002	1.00229

BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)

device	mp11	mp9	mp7
model	cmosn	cmosn	cmosn
l	1e-006	1e-006	1e-006
w	8.5e-006	5.1e-006	2e-006
m	1	1	1
ad	0	0	0
as	0	0	0
pd	8.5e-006	5.1e-006	0
ps	8.5e-006	5.1e-006	0
nrd	1	1	1
nrs	1	1	1
off	0	0	0
nqsmod	0	0	0
gmbs	7.17023e-005	5.78307e-005	4.53599e-005
gm	0.000253953	0.000206471	0.00016772
gds	1.67579e-006	1.44474e-006	1.5731e-006
vdsat	0.108797	0.134061	0.260126
vth	0.409987	0.409468	0.40731
id	1.81738e-005	1.81528e-005	3.28355e-005
vbs	-0.000123582	-0.000123439	-0.000223281
vgs	0.540377	0.580119	0.779984
vds	0.540253	0.579995	0.779761

BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)

device	m6	m5	mp13
model	cmosp	cmosp	cmosn
l	1e-006	1e-006	1e-006
w	3.36e-005	3.36e-005	2e-006
m	1	1	1
ad	7.2576e-012	7.2576e-012	0
as	7.2576e-012	7.2576e-012	0
pd	4.104e-005	4.104e-005	2e-006
ps	4.104e-005	4.104e-005	2e-006
nrd	1	1	1
nrs	1	1	1
off	0	0	0
nqsmod	0	0	0
gmbs	0.000148258	0.000148258	7.34292e-005
gm	0.000455301	0.000455301	0.000276903
gds	6.28664e-006	6.28664e-006	3.27134e-006
vdsat	0.199146	0.199146	0.443738
vth	0.417346	0.417346	0.406295
id	5.74671e-005	5.74671e-005	0.000106177
vbs	-0.00043675	-0.00043675	-0.000722001
vgs	0.654476	0.654476	1.10296
vds	0.351242	0.351242	1.10224

BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)

device	m10	m8	m7
model	cmosp	cmosp	cmosp
l	3e-007	1e-006	1e-006
w	8.1e-005	5.538e-005	5.538e-005
m	1	1	1
ad	2.9216e-011	7.2576e-012	7.2576e-012
as	2.9216e-011	7.2576e-012	7.2576e-012
pd	0.00016272	6.788e-005	6.788e-005
ps	0.00016272	6.788e-005	6.788e-005
nrd	1	1	1
nrs	1	1	1
off	0	0	0
nqsmod	0	0	0
gmbs	0.00143055	0.000189695	0.000189695
gm	0.00455263	0.000589061	0.000589061
gds	5.00628e-005	5.70122e-006	5.70122e-006
vdsat	0.198969	0.158323	0.158323
vth	0.461742	0.417344	0.417344
id	0.000572616	5.74671e-005	5.74671e-005
vbs	-0.00435188	-0.00043675	-0.00043675
vgs	0.691775	0.599016	0.599016
vds	0.849883	0.343138	0.343138

BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)

device	m6	m5	mp13
model	cmosp	cmosp	cmosn
l	1e-006	1e-006	1e-006
w	3.36e-005	3.36e-005	2e-006
m	1	1	1
ad	7.2576e-012	7.2576e-012	0
as	7.2576e-012	7.2576e-012	0
pd	4.104e-005	4.104e-005	2e-006
ps	4.104e-005	4.104e-005	2e-006
nrd	1	1	1
nrs	1	1	1
off	0	0	0
nqsmod	0	0	0
gmbs	0.000148258	0.000148258	7.34292e-005
gm	0.000455301	0.000455301	0.000276903
gds	6.28664e-006	6.28664e-006	3.27134e-006
vdsat	0.199146	0.199146	0.443738
vth	0.417346	0.417346	0.406295
id	5.74671e-005	5.74671e-005	0.000106177
vbs	-0.00043675	-0.00043675	-0.000722001
vgs	0.654476	0.654476	1.10296
vds	0.351242	0.351242	1.10224

0

BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)

device	m17	m16	m12
model	cmosp	cmosp	cmosp
l	1e-006	1e-006	3e-007
w	2.5e-005	2.5e-005	8.1e-005
m	1	1	1
ad	0	0	2.9232e-011
as	0	0	2.9232e-011
pd	2.5e-005	0	0.00016272
ps	2.5e-005	0	0.00016272
nrd	1	1	1
nrs	1	1	1
off	0	0	0
nqsmod	0	0	0
gmbs	9.63733e-005	9.64642e-005	0.00143055
gm	0.00029855	0.000298838	0.00455263
gds	1.99432e-006	1.97164e-006	5.00628e-005
vdsat	0.17276	0.172766	0.198969
vth	0.417181	0.417172	0.461742
id	3.20903e-005	3.21294e-005	0.000572616
vbs	-0.000243886	-0.000244183	-0.00435188
vgs	0.61899	0.618989	0.691775
vds	0.598965	0.618745	0.849883

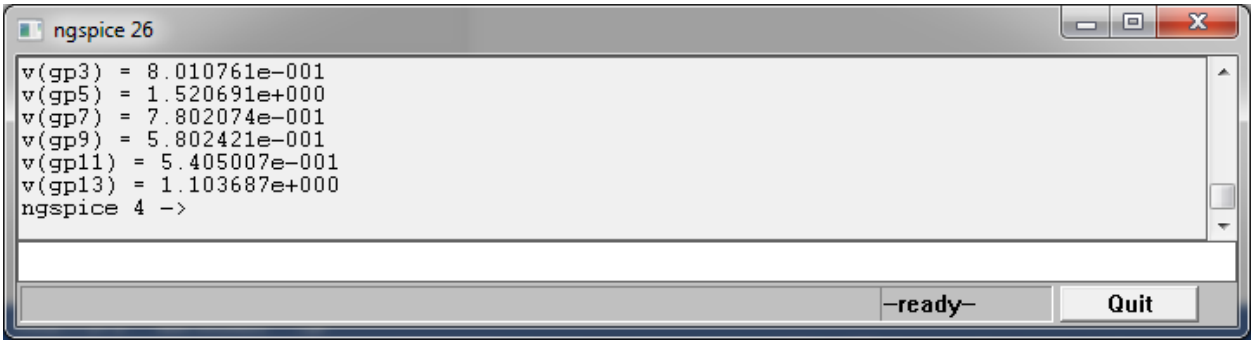
BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)

device	mp6	mp4	mp3
model	cmosp	cmosp	cmosp
l	1e-006	1e-006	1e-006
w	3.63e-006	3.37e-005	8.7e-006
m	1	1	1
ad	0	0	0
as	0	0	0
pd	3.63e-006	3.37e-005	8.7e-006
ps	3.63e-006	3.37e-005	8.7e-006
nrd	1	1	1
nrs	1	1	1
off	0	0	0
nqsmod	0	0	0
gmbs	3.4139e-005	0.00020613	8.27233e-005
gm	0.00010123	0.000545436	0.000243026
gds	1.07222e-006	0.00049808	2.6201e-006
vdsat	0.445008	0.4515	0.449431
vth	0.417049	0.417842	0.417146
id	3.28355e-005	0.000243416	7.8986e-005
vbs	-0.00024955	-0.00184997	-0.000600293
vgs	0.998674	0.997074	0.998324
vds	1.01929	0.275609	0.997723

BSIM3v1: Berkeley Short Channel IGFET Model Version-3 (3.1)

device	mp12	mp10	mp8
model	cmosp	cmosp	cmosp
l	1e-006	1e-006	1e-006
w	1.183e-005	2e-006	2e-006
m	1	1	1
ad	0	0	0
as	0	0	0
pd	1.183e-005	2e-006	0
ps	1.183e-005	2e-006	0
nrd	1	1	1
nrs	1	1	1
off	0	0	0
nqsmod	0	0	0
gmbs	0.000111348	1.87583e-005	1.87432e-005
gm	0.00032602	5.61553e-005	5.61064e-005
gds	5.71938e-006	5.26878e-007	5.34239e-007
vdsat	0.450281	0.440806	0.440791
vth	0.417339	0.4169	0.416921
id	0.000106177	1.81738e-005	1.81528e-005
vbs	-0.000806942	-0.000138121	-0.000137961
vgs	0.998117	0.998786	0.998786
vds	0.694699	1.25922	1.21948

The above ngspice result shows node voltages v(4) and v(5) of the first stage of opamp and v(9) and v(10) for the second stage.



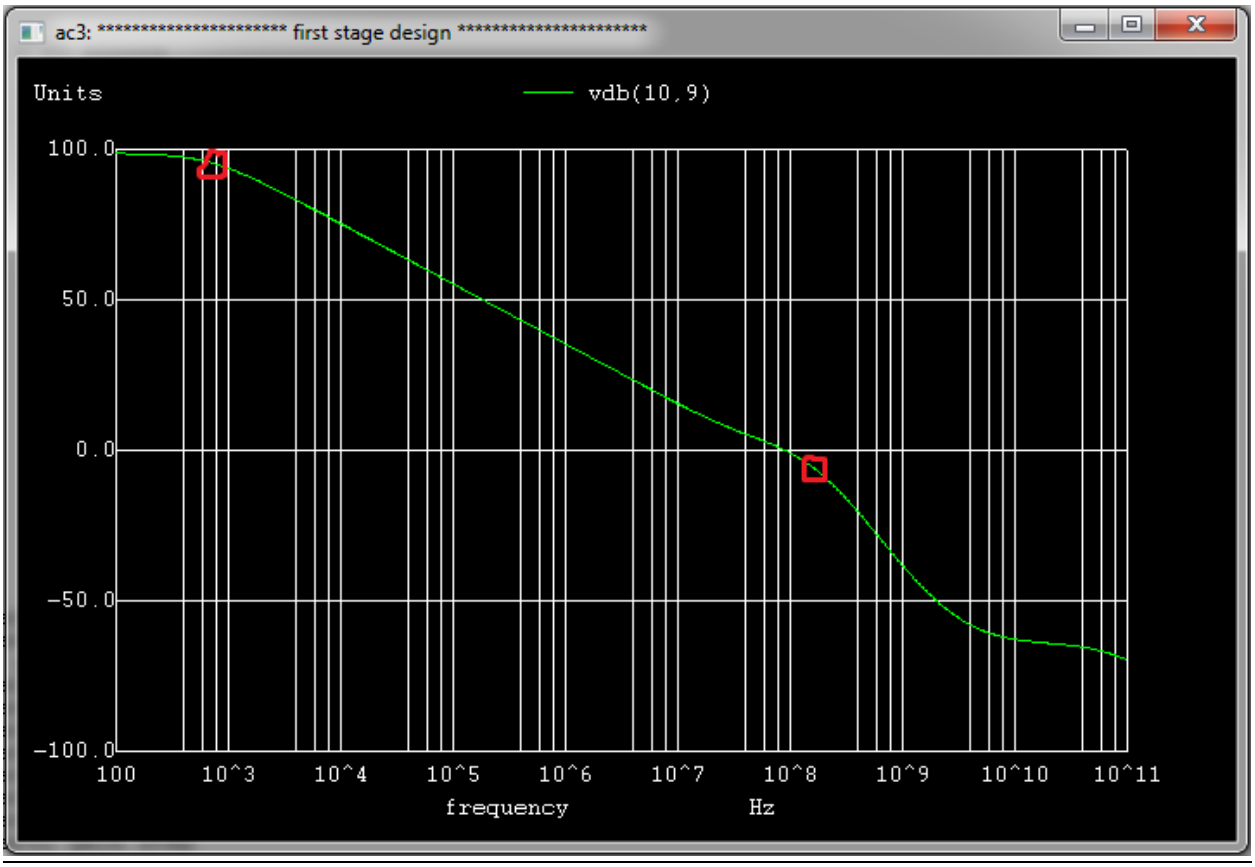
All the voltages shown above are the bias voltages given by reference generator to OpAmp and CMFB.

➢ Section 6:

AC Simulation Results

Netlist

Magnitude Plot of Open loop differential voltage gain in dB



The above plot highlights the location of dominant pole and the third pole, the second pole being compensated by a zero.

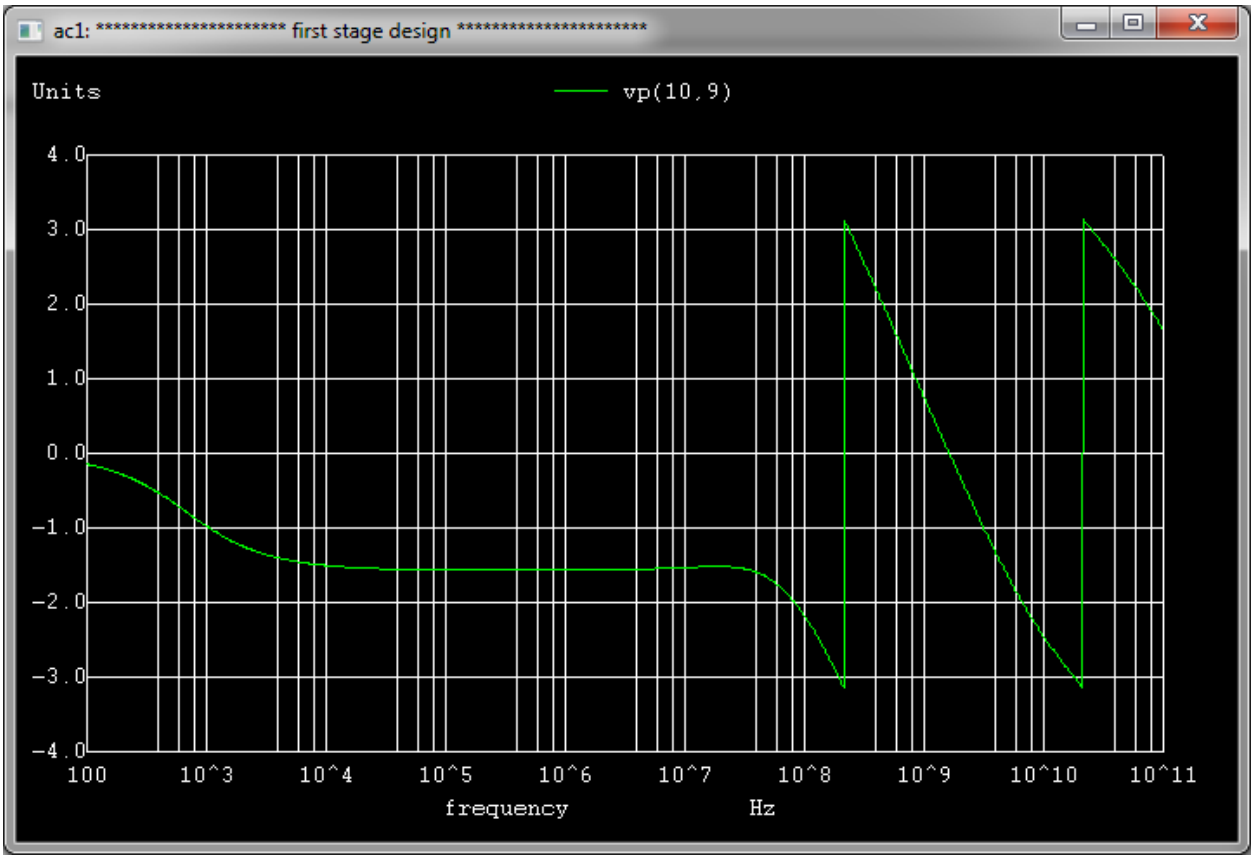
Pole1 =500Hz

Pole3 = 105MHz

Magnitude of open loop differential voltage gain in dB = 98.275dB

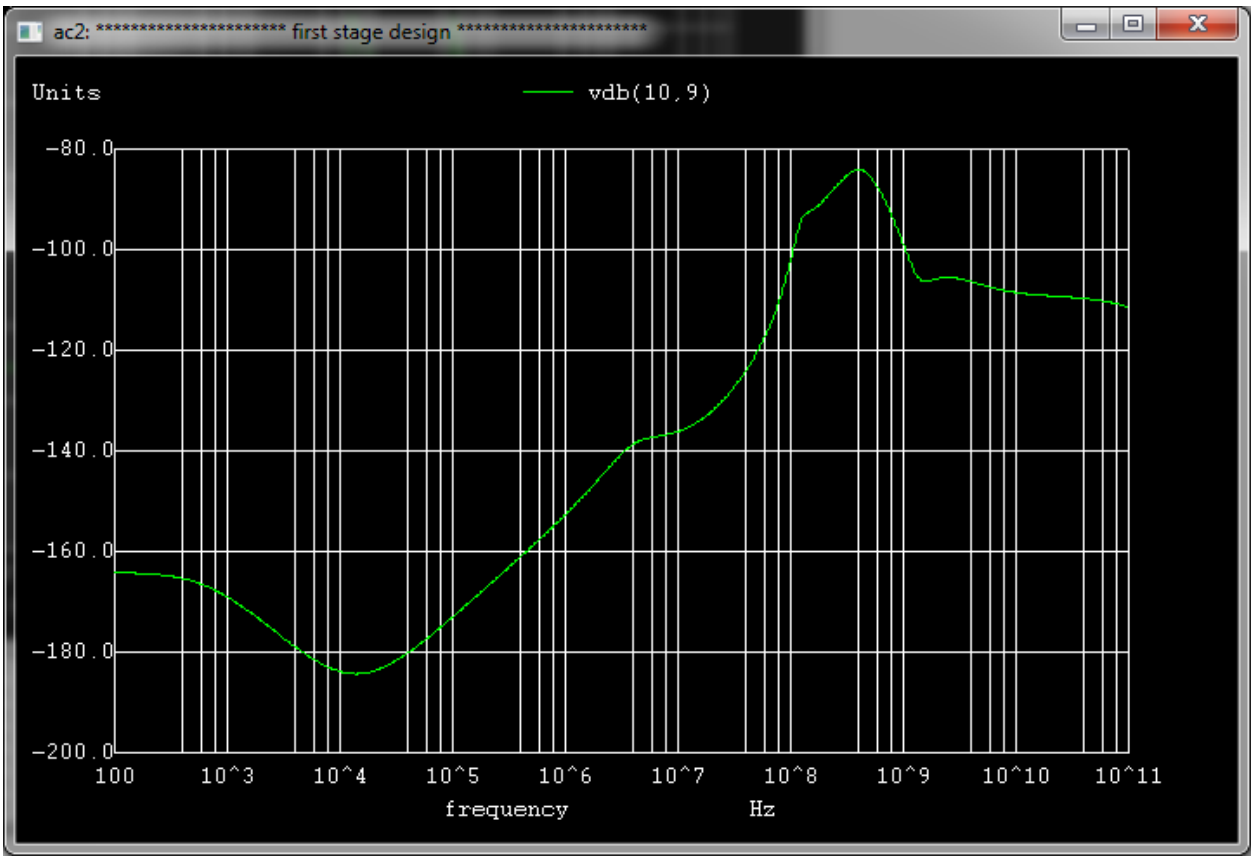
Unity Gain Bandwidth = 89.05 MHz

Phase Plot:



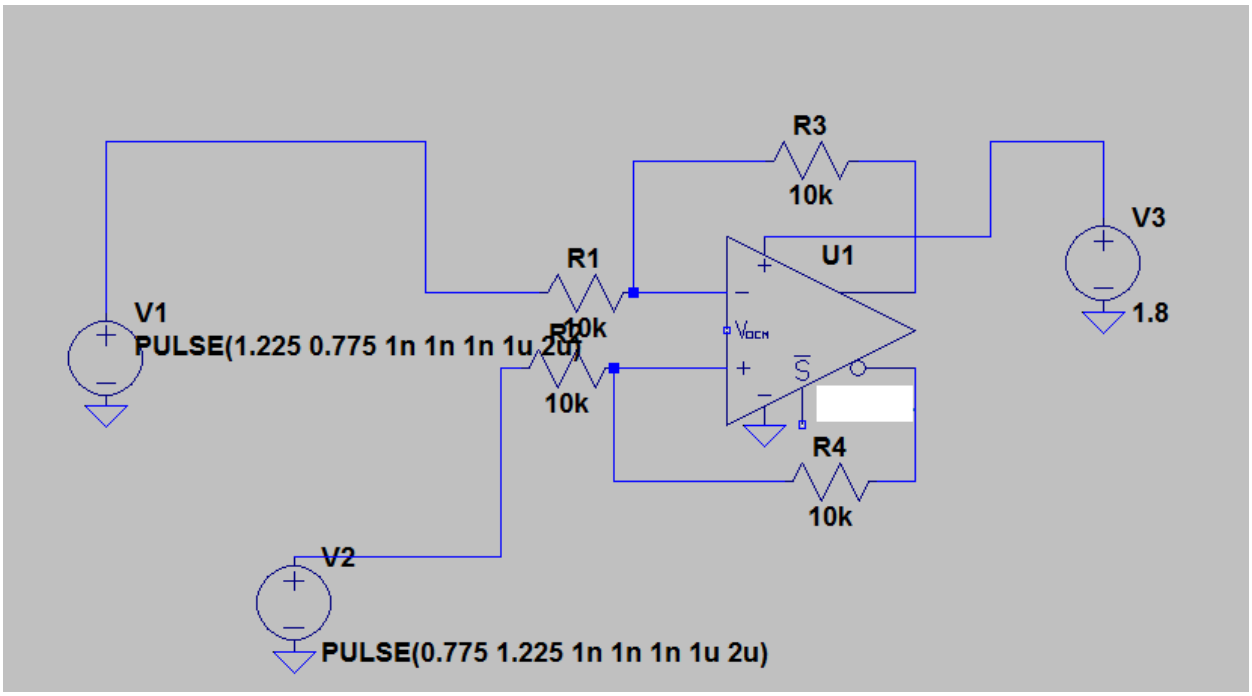
Phase Margin = -1.988 * 180 / π + 180 = 66.09 degrees

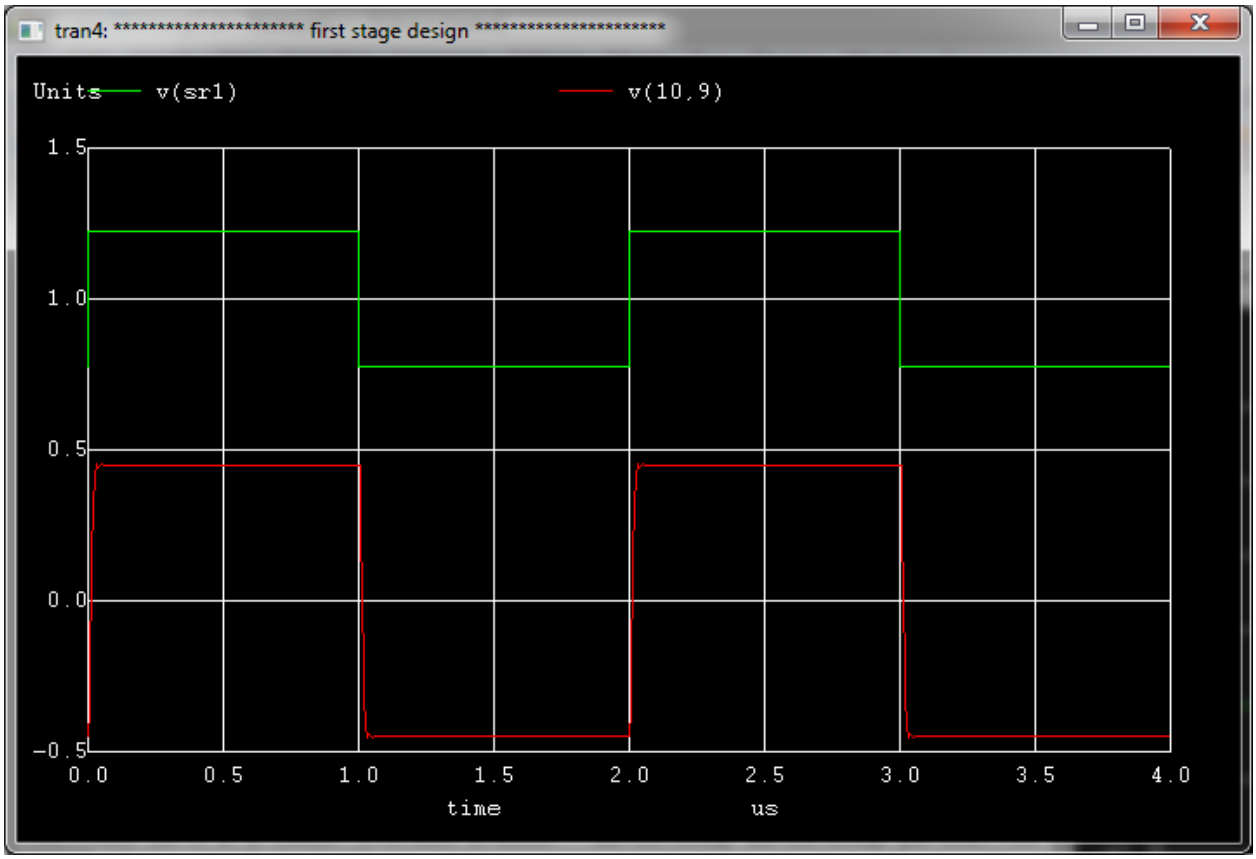
Magnitude Plot of Open loop common-mode voltage gain in dB, as a function of frequency

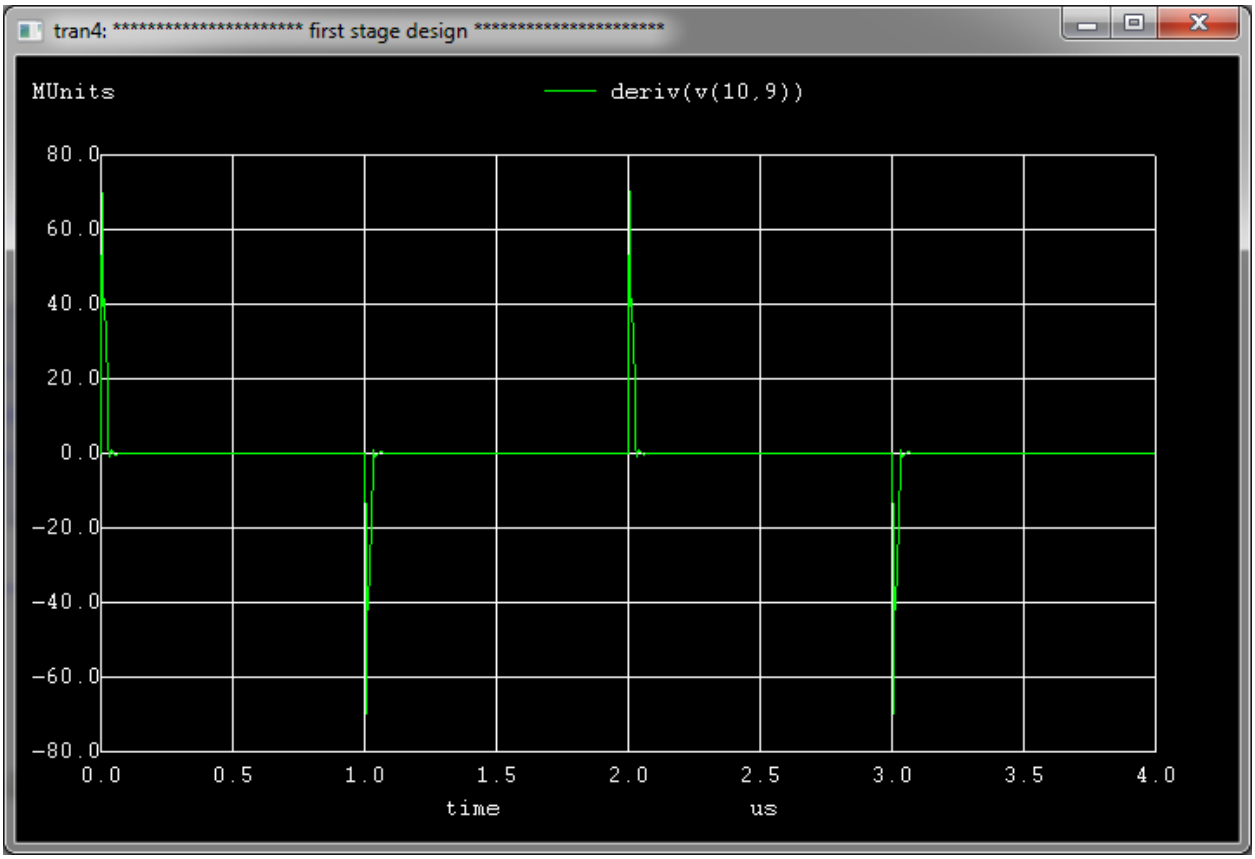


➢ Section 7:

Simulation results of slew rate and step response to +450 mV and -450 mV differential input step voltage in closed loop mode with voltage gain of -1




tran4: ********** first stage design **********
Units
v(sr1)
v(10,9)
1.5
1.0
0.5
0.0
-0.5
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
time
us



From above graph, **Slew Rate is = 68V/uS**

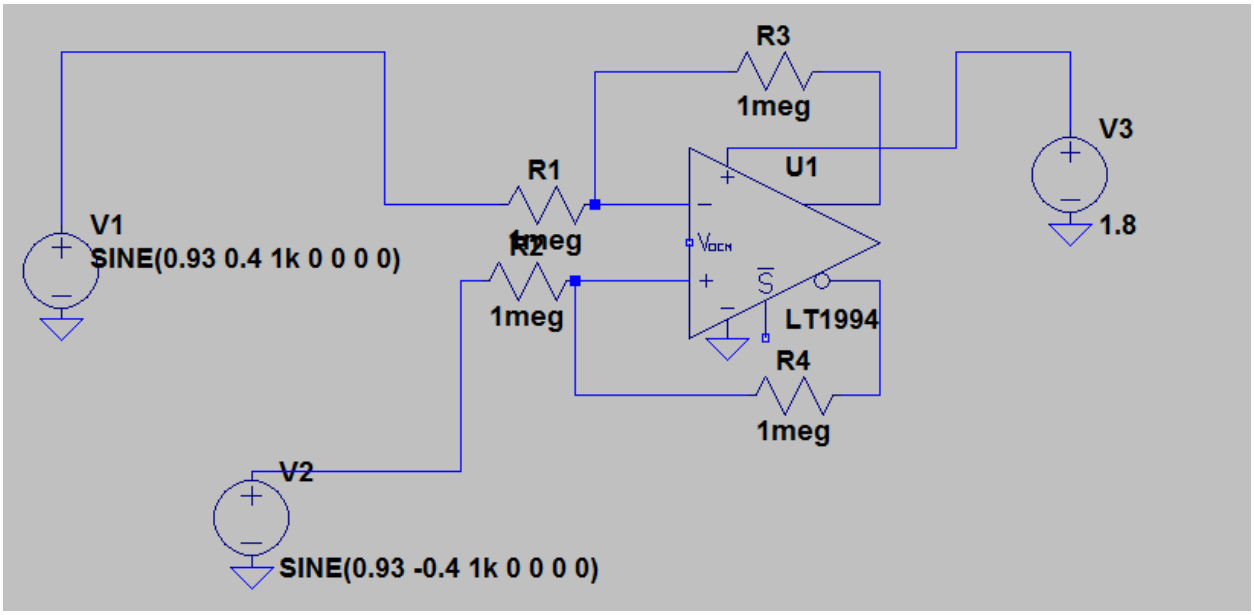
Slew Rate

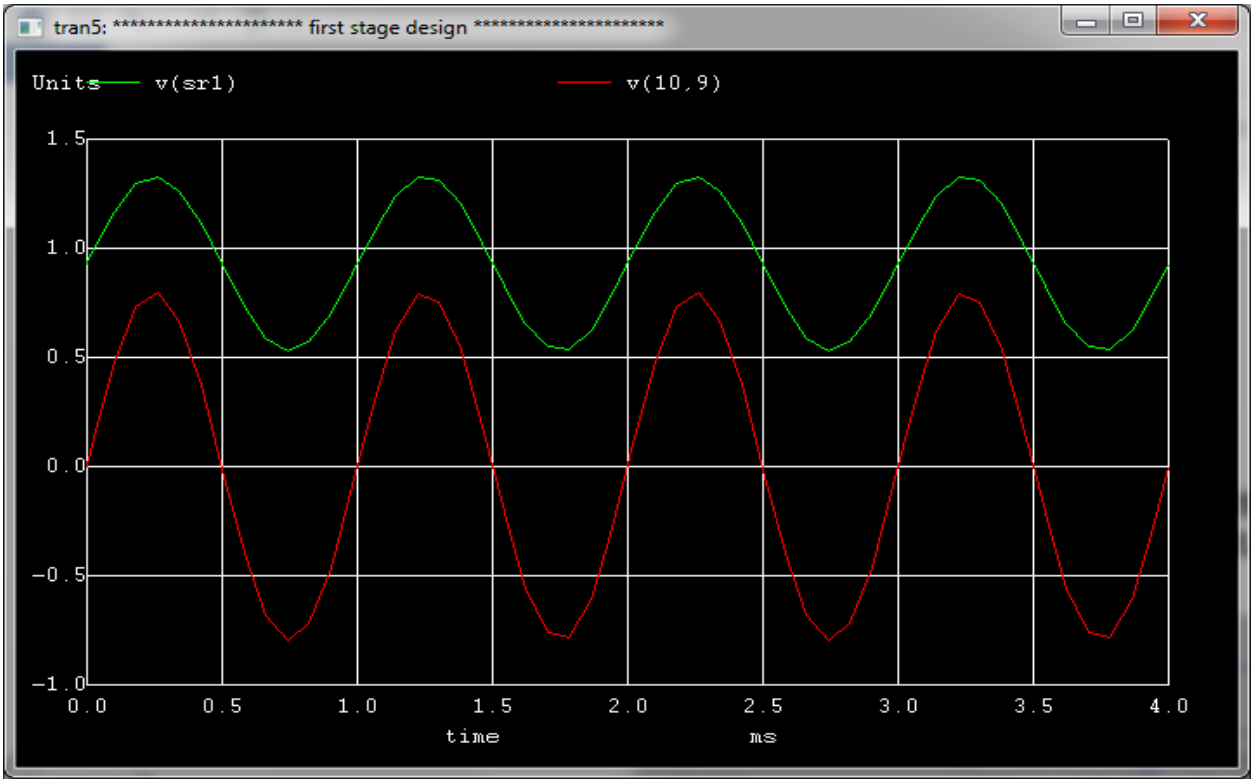
Partial netlist for slew rate

```
Rs1 sr1 g1 1meg
Rs2 sr2 g2 1meg
Rs3 g1 9 1meg
Rs4 g2 10 1meg

Vsr1 sr1 0 pulse(0.775 1.225 1n 1n 1n 1u 2u)
Vsr2 sr2 0 pulse(1.225 0.775 1n 1n 1n 1u 2u)

.tran 0 4u
.control
Run

plot v(sr1) v(10,9)
plot deriv(v(10,9))
.endc
.end
```

➢ Section 8:

Transient simulation for maximum output voltage swing in closed loop mode.





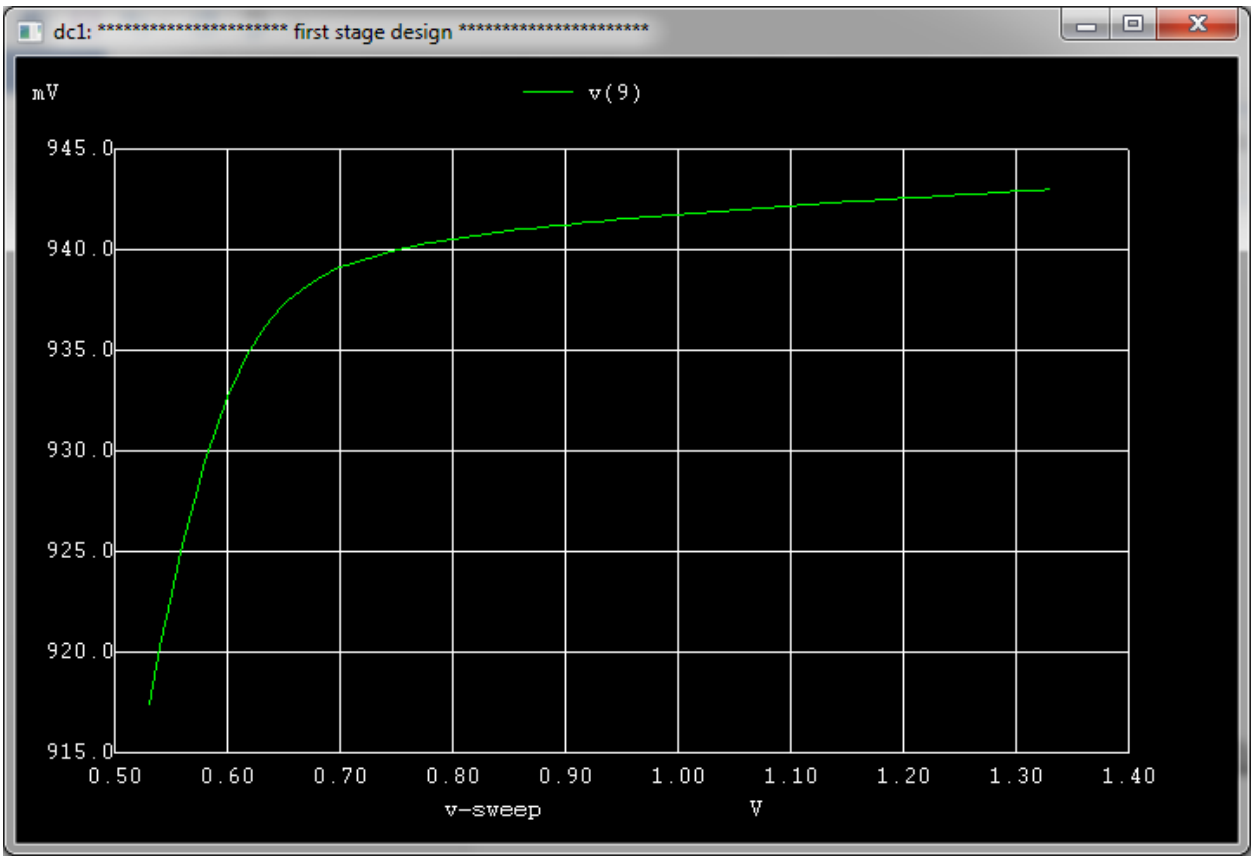
Partial Netlist for Output Swing

```
Rs1 sr1 g1 1meg
Rs2 sr2 g2 1meg
Rs3 g1 9 1meg
Rs4 g2 10 1meg

Vsr1 sr1 0 sin(0.93 0.4 1k 0 0)
Vsr2 sr2 0 sin(0.93 -0.4 1k 0 0)
.tran 0 4m
.control
run

plot v(sr1) v(10,9)

.endc
.end
```

From simulation we see that closed loop unity gain is achieved along with the swing of 1.6V

➢ Section 9:

Common-mode (CM) DC simulation



From the above graph, it can be inferred that the output is stable from 0.7v to 1.4v and its variation is less with input voltage.